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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/525,173	02/22/2005	Nigel D. Young	GB 020139	7743

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P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
MALDONADO, JULIO J	

ART UNIT	PAPER NUMBER
2823	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/525,173	YOUNG, NIGEL D.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 19-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,8 and 13-15* is/are rejected.

7)☒ Claim(s) *2-7,9-12 and 19-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. The indicated allowability of claim 1 is withdrawn in view of the newly discovered reference(s) to Antonuk et al. (U.S. 5,079,426) in view of Kusumoto et al. (U.S. 6,027,960). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 8 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Antonuk et al. (U.S. 5,079,426, hereinafter Antonuk) in view of Kusumoto et al. (U.S. 6,027,960, hereinafter Kusumoto) and Wolf et al. (Silicon Processing for the VLSI Era, Volume 1: Process Technology, hereinafter Wolf).

Antonuk (Figs.1-2) teaches a method of manufacturing thin-film circuit elements that include a diode integrated with a crystalline thin-film transistor (52) including the steps of forming on a circuit substrate (12) an active film (22, 25, 27, 28); forming doped source and drain regions (25, 29) of the transistor at ends of a channel area; providing an interconnection electrode film (22) between an electrode area of the thin film transistor (52) and a diode area over which the diode (30) on which the active film for the diode is to be deposited; and forming said diode (30) over the interconnection film (22), wherein the diode (30) is formed after forming the active film (22, 25, 27, 28),

wherein said diode (30) is a PIN diode, and wherein said thin film transistor is made of crystalline silicon (Antonuk, column 4, line 54 – column 6, line 10).

Antonuk fails to disclose wherein active semiconductor film and the source and drain regions are formed at temperatures higher than the diode film.

Kitakado (Figs.1A-4) teaches a method to form thin-film circuit elements that include a crystalline thin-film transistor including the steps of forming on a circuit substrate (101) a crystalline silicon active film (107), wherein said forming of said crystalline silicon active film further includes laser crystallization; forming a source/drain regions (113, 114) in the crystalline active film (107) involving temperatures between 300°C to 650°C; forming an insulating film (108) over said crystalline film (107); and performing a hydrogenation step to the crystalline active semiconductor film (107) (Kitakado, column 6, line 4 – column 8, line 65).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Antonuk and Kitakado to enable forming the crystalline semiconductor film and the source drain/regions of Antonuk according to the teachings of Kitakado because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods of forming the disclosed crystalline semiconductor film and source/drain regions of Antonuk and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

It would also have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Antonuk and Kitakado to enable

performing the hydrogenation step on the active crystalline semiconductor film of Antonuk according to the teachings of Kitakado for the further advantage of terminating the dangling bonds in the active layer by thermally excited hydrogen (Kitakado, column 8, lines 50 – 65).

The combined teachings of Antonuk and Kitakado fail to expressly disclose a process temperature for the formation of the active crystalline semiconductor film.

However, Kusumoto (Figs.2A-2F) teaches a method of manufacturing thin-film circuit elements that include a crystalline thin-film transistor including the steps of forming an active crystalline semiconductor film (203) including the steps of depositing an amorphous silicon layer on a substrate (201); and laser annealing said amorphous silicon layer at a temperature of 600°C to form said active crystalline semiconductor film (203) (Kusumoto, column 6, line 53 – column 7, line 19).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Antonuk and Kitakado with Kusumoto to enable forming the crystalline semiconductor film of Antonuk and Kitakado according to the teachings of Kusumoto because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods of forming the disclosed crystalline semiconductor film of Antonuk and Kitakado and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

The combined teachings of Antonuk, Kitakado and Kusumoto fail to disclose a deposition temperature for the PIN diode. However, the combined teachings of

Antonuk, Kitakado and Kusumoto disclose wherein said PIN diode is made of amorphous silicon (Antonuk, column 5, lines 17 – 25).

Furthermore, Wolf discloses forming amorphous silicon at temperatures below 580°C (Wolf, page 179).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Antonuk, Kitakado and Kusumoto with Wolf to enable forming the amorphous silicon used for the PIN diode Antonuk, Kusumoto and Kitakado at the deposition temperatures disclosed in Wolf because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods of forming the diode of Antonuk, Kusumoto and Kitakado and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the teachings of Antonuk, Kusumoto, Kitakado and Wolf to form the crystalline semiconductor film and the source/drain regions at the recited temperature differences to arrive at the claimed invention.

The combined teachings of Antonuk, Kitakado, Kusumoto and Wolf fail to disclose forming the PIN diode by depositing an active semiconductor film for the diode and etching away the active semiconductor film for the diode from over the etch-stop film to leave the active semiconductor film for the diode over the interconnection film in the diode area.

However, Wei (Figs.1a-1b) teaches a method of manufacturing thin-film circuit elements that include a diode (145) integrated with a crystalline thin-film transistor including the steps of forming a metal conductive region (120) over a substrate (105); etching said metal conductive region to form an electrode (124); forming an active semiconductor film for the PIN diode (145) on said conductive region (120); and etching away the active semiconductor film for the PIN diode (145) stopping at the conductive region (120) and the substrate (105) to from said PIN diode (145) (Wei, column 3, line 47 – column 4, line 60).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Antonuk, Kitakado, Kusumoto and Wolf with Wei to enable the disclosed forming the interconnection electrode of Antonuk, Kitakado, Kusumoto and Wolf according to the teachings of Wei because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods of performing the disclosed interconnection electrode of Antonuk, Kitakado, Kusumoto and Wolf and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

It would also have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Antonuk, Kitakado, Kusumoto and Wolf with Wei to enable forming the PIN diode of Antonuk, Kitakado, Kusumoto and Wolf by forming an active semiconductor material for a diode and etching down to the interconnection of the combined teachings of Antonuk, Kitakado and Kusumoto according to the teachings of Wei because one of ordinary skill in the art would have

been motivated to look to analogous art teaching alternative suitable or useful methods of forming the disclosed PIN diode of Antonuk, Kitakado, Kusumoto and Wolf and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Accordingly, one of ordinary skill in the art at the time the invention was made to use interconnection of the combined teachings of Antonuk, Kitakado, Kusumoto, Wolf and Wei to arrive at the claimed invention.

Allowable Subject Matter

4. Claims 2-7 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter:

Antonuk (Figs.1-2) teaches a method of manufacturing thin-film circuit elements that include a diode integrated with a crystalline thin-film transistor (52) including the steps of forming on a circuit substrate (12) an active film (22, 25, 27, 28); forming doped source and drain regions (25, 29) of the transistor at ends of a channel area; providing an interconnection electrode film (22) between an electrode area of the thin film transistor (52) and a diode area over which the diode (30) on which the active film for the diode is to be deposited; and forming said diode (30) over the interconnection film (22), wherein the diode (30) is formed after forming the active film (22, 25, 27, 28),

wherein said diode (30) is a PIN diode, and wherein said thin film transistor is made of crystalline silicon (Antonuk, column 4, line 54 – column 6, line 10).

However, Antonuk fails to disclose wherein the etch-stop film an insulating film that extends over the interconnection film and that has a window at the diode area to permit contact between the interconnection film and the active semiconductor film of the diode as disclosed in claim 2.

6. Claims 9-12, 20 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

Antonuk (Figs.1-2) teaches a method of manufacturing thin-film circuit elements that include a diode integrated with a crystalline thin-film transistor (52) including the steps of forming on a circuit substrate (12) an active film (22, 25, 27, 28); forming doped source and drain regions (25, 29) of the transistor at ends of a channel area; providing an interconnection electrode film (22) between an electrode area of the thin film transistor (52) and a diode area over which the diode (30) on which the active film for the diode is to be deposited; and forming said diode (30) over the interconnection film (22), wherein the diode (30) is formed after forming the active film (22, 25, 27, 28), wherein said diode (30) is a PIN diode, and wherein said thin film transistor is made of crystalline silicon (Antonuk, column 4, line 54 – column 6, line 10).

However, Antonuk fails to disclose wherein the interconnection film is connected to a PIN diode and furthermore, wherein at least a portion of the etch-stop interconnection film is provided on a gate-dielectric film on the crystalline active semiconductor film to form a top gate electrode of the transistor as disclosed in claim 9.

Conclusion

8. Applicants are encouraged, where appropriate, to check Patent Application Information Retrieval (PAIR) (http://portal.uspto.gov/external/portal/pair) which provides applicants direct secure access to their own patent application status information, as well as to general patent information publicly available.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax number for this group is 571-273-8300. Updates can be found at http://www.uspto.gov/web/info/2800.htm.

Julio J. Maldonado
Patent Examiner
Art Unit 2823

Julio J. Maldonado
January 11, 2008

GEORGE R. FOURSON
PRIMARY EXAMINER